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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/580,505	05/23/2006	Jens Kristian Poulsen	47161-00047USPX	2345

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EXAMINER	
ROBINSON, RYAN C	
ART UNIT	PAPER NUMBER
2614	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/580,505	POULSEN, JENS KRISTIAN	
	Examiner	Art Unit	
	RYAN C. ROBINSON	2614	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 July 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1*-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 May 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *5/23/2006; 7/24/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The Art Unit location of your application in the PTO has changed. To aid in correlating any papers for this application, all further correspondence regarding this application should be directed to Group Art Unit **2614**.

2. This communication is responsive to the applicant's response/amendment filed on 7/25/2008.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the DC voltage generating means disposed within the microphone housing, operatively coupled to the clock signal, as claimed in claim 5, must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for

consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

4. Claim 5 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 5 discloses a "DC voltage generating means disposed within the microphone housing", implying that a DC voltage is generated within the digital microphone housing from an internal power source, while simultaneously disclosing that the "DC voltage supply" is derived from the clock signal. It is unclear whether the DC voltage generating means is a component for deriving a DC voltage, or a voltage supply. For the purpose of examination, examiner reads "DC voltage generating means" as a means to derive a DC voltage from a clock signal.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-2 and 4-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Deruginsky et al., U.S. Publication No. 2003/0223592, filed on 4/10/2002, (hereby Deruginsky), in view of Fujimori et al., U.S. Patent No. 6,326,912, published on 12/4/2001, (hereby Fujimori).

7. As to claim 1, Deruginsky teaches a digital microphone (Fig. 2, element 103) comprising: a microphone housing (104) having a sound inlet (106), and comprising: a transducer element (108) comprising a displaceable diaphragm (Para. 0015, lines 1-4), and adapted to generate a transducer signal representative of sound (Para. 0015, lines 4-6) received through the sound inlet (106), an analog-to-digital converter (12), and an externally accessible terminal (120) adapted to provide an unformatted single-bit output signal (Para. 0056, lines 1-3). It is noted that Derunginsky does not teach a multi-level quantizer operatively coupled to the transducer element to convert the transducer signal into multi-bit samples representative of the transducer signal, and a digital signal converter adapted to convert the multi-bit samples into a single-bit output signal. However, Derunginsky teaches that the analog-to-digital converter is preferably a sigma-delta modulator with a single-bit output, but is not restricted to a particular analog-to-digital converter (Para. 0045, lines 1-6).

Fujimori teaches an improved analog to digital converter, which employs a multi-level quantizer (Fig. 3, element 16), to convert the transducer signal into multi-bit

samples, and a digital signal converter (18) adapted to convert the multi-bit samples into a single-bit output (Col. 3, line 67; Col. 4, lines 1-2). Therefore, it would have been obvious to one of ordinary skill to incorporate the analog-to-digital converter taught by Fujimori, as a suitable analog to digital converter in the microphone taught by Deruginsky, in order to take advantage of a multi bit quantizer, while having a single bit output, thereby reducing the noise and complexity of the analog-to-digital converter (Col. 3, lines 23-29).

8. As to claim 2, Fujimori teaches that the analog-to-digital converter comprises an oversampled delta-sigma modulator (Col. 1, lines 25-26).

9. As to claims 4 and 5, Deruginsky teaches that the microphone housing comprises a second externally accessible terminal for receipt of an external clock signal (Para. 0022, liens 2-3), and voltage generating means disposed within the microphone housing and operatively coupled to the external clock signal so as to derive a DC voltage supply for operating at least the analog-to-digital converter (Para. 0030).

10. As to claim 6, both Deruginsky and Fujimori do not explicitly teach a range of discrete quantization levels in the multi-level quantizer. However, Fujimori does not restrict the quantity of levels to a specific number or range. Furthermore, Fujimori teaches that increasing the number of bits used in the quantizer, which is in effect, increasing the number of quantization levels, exponentially reduces noise. Therefore, it

would have been obvious to one of ordinary skill to provide the multi-level quantizer in the combination of Derunginsky and Fujimori with an adequate number of discrete quantizer levels, including between 3 and 64 discrete quantizer levels.

11. As to claim 7, Fujimori teaches that the multi-bit samples provided by the analog-to-digital converter are represented in two's complement format (Fig. 9, element 80a). The input to the adder 80a, denoted my "M-BIT" is in two's complement format.

15. As to claim 8, Fujimori discloses that the multi-bit samples generated by the multi-level quantizer (Col. 4, lines 1-2), are represented by a set of corresponding symbols, and wherein each symbol comprises a number of one signs which is proportional with a magnitude of the corresponding multi-bit sample (Col. 6, lines 3-5). Fujimori teaches that the stream of 1's and 0's is dependent on the magnitude of the analog signal, corresponding to a number of one signs which is proportional with a magnitude.

12. As to claim 9, both Deruginsky and Fujimori do not explicitly teach a range of discrete quantization levels in the multi-level quantizer. However, Fujimori does not restrict the quantity of levels to a specific number or range. Furthermore, Fujimori teaches that increasing the number of bits used in the quantizer, which is in effect, increasing the number of quantization levels, exponentially reduces noise. Therefore, it would have been obvious to one of ordinary skill to provide the multi-level quantizer in

the combination of Derunginsky and Fujimori with an adequate number of discrete quantizer levels, including between 3 and 5 discrete quantizer levels.

13. As to claim 10, both Deruginsky and Fujimori do not explicitly teach a range of discrete quantization levels in the multi-level quantizer. However, Fujimori does not restrict the quantity of levels to a specific number or range. Furthermore, Fujimori teaches that increasing the number of bits used in the quantizer, which is in effect, increasing the number of quantization levels, exponentially reduces noise. Therefore, it would have been obvious to one of ordinary skill to provide the multi-level quantizer in the combination of Derunginsky and Fujimori with an adequate number of discrete quantizer levels, including N levels, each corresponding symbol comprising N-1 bits; N being an integer between 3 and 17.

14. As to claim 11, Fujimori teaches a digital signal converter (Fig. 3, element 24), comprising a delay circuit (Col. 1, lines 49-51), FIR filter corresponding to a delay circuit, in cascade with an integer ratio upsampler (Col. 1, lines 48-49). There is an interpolator (24) which increases the sampling frequency, corresponding to an upsampler.

15. As to claim 12, Deruginsky teaches a preamplifier (110) interposed between the transducer element and the analog to digital converter.

16. As to claim 13, Fujimori teaches an interpolator (24) operatively coupled between the multi-bit samples provided by the analog-to-digital converter (16) and the digital signal converter (18).

17. As to claim 14, Deruginsky teaches a portable communication device (2) comprising digital microphone (3).

18. As to claim 15, Deruginsky teaches a monolithic integrated circuit (Para. 0025, lines 1-4) for a miniature microphone, comprising a preamplifier (110) adapted to provide an amplified transducer signal and comprising an input section couplable to a miniature electret or condenser transducer element (108), an analog-to-digital converter (112), operatively coupled to the amplified transducer signal, and an integrated circuit pad adapted to provide the single bit output signal (20). It is noted that Deruginsky does not teach a multi-level quantizer operatively coupled to the amplified transducer signal and adapted to convert the amplified transducer signal into multi-bit samples representative of the amplified transducer signal, and a digital signal converter adapted to convert the mult-bit samples into an unformatted single-bit output signal. However, Derunginsky teaches that the analog-to-digital converter is preferably a sigma-delta modulator with a single-bit output, but is not restricted to a particular analog-to-digital converter (Para. 0045, lines 1-6).

Fujimori teaches an improved analog to digital converter, which employs a multi-level quantizer (Fig. 3, element 16), to convert the transducer signal into multi-bit

samples, and a digital signal converter (18) adapted to convert the multi-bit samples into a single-bit output (Col. 3, line 67; Col. 4, lines 1-2). Therefore, it would have been obvious to one of ordinary skill to incorporate the analog-to-digital converter taught by Fujimori, as a suitable analog to digital converter in the microphone taught by Deruginsky, in order to take advantage of a multi bit quantizer, while having a single bit output, thereby reducing the noise and complexity of the analog-to-digital converter (Col. 3, lines 23-29).

19. As to claim 16, Fujimori teaches that the multi-bit samples generated by the multi-level quantizer (Col. 4, lines 1-2), are represented by a set of corresponding symbols, and wherein each symbol comprises a number of one signs which is proportional with a magnitude of the corresponding multi-bit sample (Col. 6, lines 3-5). Fujimori teaches that the stream of 1's and 0's is dependent on the magnitude of the analog signal, corresponding to a number of one signs which is proportional with a magnitude.

20. As to claim 17, Fujimori teaches that the analog-to-digital converter comprises an oversampled delta-sigma modulator (Col. 1, lines 25-26).

21. As to claim 18, both Deruginsky and Fujimori do not explicitly teach a number of discrete quantization levels in the multi-level quantizer. However, Fujimori does not restrict the quantity of levels to a specific amount. Furthermore, Fujimori teaches that

increasing the number of bits used in the quantizer, which is in effect, increasing the number of quantization levels, exponentially reduces noise. Therefore, it would have been obvious to one of ordinary skill to provide the multi-level quantizer in the combination of Derunginsky and Fujimori with an adequate number of discrete quantizer levels, including 3 or 5 discrete quantizer levels.

22. As to claim 19, Fujimori teaches that the digital signal converter (18) is a sigma-delta converter

23. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Deruginsky et al., U.S. Publication No. 2003/0223592, filed on 4/10/2002, (hereby Deruginsky), Fujimori et al., U.S. Patent No. 6,326,912, published on 12/4/2001, (hereby Fujimori), further in view of Feste et al, U.S. Patent No. 5,886,656, published on 3/23/1999, (hereby Feste).

24. As to claim 3, both Deruginsky and Fujimori do not teach an integral clock generator operatively coupled to the analog-to-digital converter and the digital signal converter. However digital microphones with an integral clock are well known in the art, and Feste teaches a digital microphone (Fig. 1) with an integral clock (T) generator operatively coupled to the analog-to-digital converter (C) and the digital signal converter (OUT). Therefore, it would have been obvious to one of ordinary skill in the art to provide an integral clock in the combination of Derugninsky and Fujimori as an optional

design choice, with the predicable benefit of not having to rely on an external clock source.

Response to Arguments

25. Applicant's arguments with respect to claims 1-19 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record

a.	US Publication Number	**2003/0223592**
b.	US Patent Number	**6,326,912**
c.	US Patent Number	**5,886,656**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan C. Robinson whose telephone number is (571) 270-3956. The examiner can normally be reached on Monday through Friday from 9 am to 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Suhan Ni, can be reached on (571) 272-7505. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ryan Robinson

/Suhan Ni/

Primary Examiner, Art Unit 2614